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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,416	DORIS ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments filed 12/29/06 have been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al (US 2005/0285187 A1) in view of De Souza et al (US 2005/0116290 A1).

2. Regarding claim 1, Bryant et al discloses a semiconductor device structure comprising: a plurality of nFETs (Figure 4, reference 20), a plurality of pFETs (Figure 4, reference 45), and wherein a gate electrode orientation is such that the nFETs and the pFETs are substantially parallel to each other (Figure 4, reference 5). However, Bryant et al does not disclose at least two active regions having different surface directions.

De Souza et al discloses at least two active regions having different surface directions (Figure 6, references 170 and 180).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bryant et al, with the teachings of De Souza et al, for the purpose of utilizing localized amorphization and recrystallization of stacked template layers for making a planar substrate having semiconductor layers of different crystallographic orientations.

3. Regarding claim 2, Bryant et al discloses wherein the pFETs are located in an active region with a current flow in a <11 0> surface direction, and the nFETs are located in an active region with a current flow in a <1 00> surface direction (Figure 4).

4. Regarding claim 3, Bryant et al discloses wherein the pFETs are located in an active region with a (11 0) surface orientation and a <111 > surface direction, and the nFETs are located in an active region with a (1 00) surface orientation and a <110> surface direction (Figure 4).

5. Regarding claim 4, Bryant et al discloses further comprising means for applying: a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction with respect to a current flow of the nFET (Figure 4, references 25 and 55); and a tensile stress in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET (pg.5, paragraph 0077).

Claims 5 and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al (US 2005/0285187 A1) in view of De Souza et al (US 2005/0116290 A1).

6. Regarding claim 5, Bryant et al discloses a method of forming a semiconductor device structure, the method comprising the steps of: bonding a first wafer having a first surface direction atop a second wafer having a different second surface direction (Figure 4, references 9, 15 and 17) and forming an opening through the first wafer to the second wafer (Figure 4, reference 70). However, Bryant et al does not disclose forming a region in the opening coplanar with a surface of the first wafer, wherein the region has the second surface direction.

De Souza et al discloses forming a region in the opening coplanar with a surface of the first wafer, wherein the region has the second surface direction (Figure 6, references 170 and 180).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bryant et al, with the teachings of De Souza et al, for the purpose of utilizing localized amorphization and recrystallization of stacked template layers for making a planar substrate having semiconductor layers of different crystallographic orientations.

7. Regarding claim 10, Bryant et al discloses wherein each wafer includes a silicon layer on an insulator layer (Figure 4, references 9, 15 and 17), and the opening forming step includes forming the opening to the silicon layer of the second wafer (Figure 4, reference 70).

8. Regarding claim 11, Bryant et al discloses wherein the region forming step includes epitaxially growing silicon in the opening, and planarizing the silicon (pg.4, paragraph 0064).

9. Regarding claim 12, Bryant et al discloses wherein the opening forming step includes forming a sidewall spacer along the opening (Figure 4, reference 4).

10. Regarding claim 13, Bryant et al discloses wherein the first surface direction is a <100> surface direction and the second surface direction is a <110> surface direction (Figure 4).

11. Regarding claim 14, Bryant et al discloses wherein the first surface direction is a <110> surface direction and the second surface direction is a <111 > surface direction (Figure 4).

12. Regarding claim 15, Bryant et al discloses wherein the first wafer has a first surface orientation and the second wafer has a different second orientation, and the region has the second surface orientation (Figure 4).

13. Regarding claim 16, Bryant et al discloses wherein the first surface direction and the second surface direction are selected to degrade mobility (Figure 4).

Claims 6-9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al (US 2005/0285187 A1) and De Souza et al (US 2005/0116290 A1) in view of Machesney et al (5,670,388).

14. Bryant et al discloses all above claimed subject matter except implanting oxygen and annealing to form a buried oxide layer (claims 6 and 18).

Machesney et al discloses implanting oxygen and annealing to form a buried oxide layer (column 8, lines 35-54).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bryant et al and De Souza et al, with the teachings of Machesney et al, for the purpose of forming a body substrate connector for an SOI FET.

15. Regarding claim 7, Bryant et al discloses further comprising the step of forming a first type gate electrode on the region, and a second type gate electrode on another region of the first wafer, and all of the gate electrodes are substantially parallel to one another (Figure 4, reference 5).

16. Regarding claim 8, Bryant et al discloses wherein the first gate electrode includes a pFET (Figure 4, reference 45), and the second gate electrode includes an nFET (Figure 4, reference 20).

17. Regarding claim 9, Bryant et al discloses further comprising the step of applying at least one of a filled trench configuration and at least one film to provide: a compressive stress in a longitudinal direction with respect to a current flow of the pFET and a transverse direction

with respect to a current flow of the nFET (Figure 4, references 25 and 55); and a tensile stress applied in a longitudinal direction with respect to a current flow of the nFET and a transverse direction with respect to a current flow of the pFET (pg.5, paragraph 0077).

Claims 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al (US 2005/0285187 A1) in view of De Souza et al (US 2005/0116290 A1).

18. Regarding claim 17, Bryant et al discloses a method of forming a semiconductor device structure, the method comprising the steps of: forming an opening through the first wafer to a silicon layer of the second wafer (Figure 4, reference 70); generating a silicon in the opening to a surface of the first wafer, wherein the silicon has the different second surface orientation (Figure 4); forming a plurality of pFETs on the silicon (Figure 4, reference 45), and a plurality of nFETs on another region of the first wafer (Figure 4, reference 20), wherein gate electrodes of the FETs are substantially parallel to one another (Figure 4, reference 5); and applying at least one of a filled trench configuration and at least one process to provide (Figure 4, reference 70): a compressive stress in a longitudinal direction with respect to a current flow of the pFETs and a transverse direction with respect to a current flow of the nFETs (Figure 4, reference 55); and a tensile stress in a longitudinal direction with respect to a current flow of the nFETs and a transverse direction with respect to a current flow of the pFETs (pg.5, paragraph 0077). However, Bryant et al does not disclose bonding a first wafer having a first surface direction and a first surface orientation atop a second wafer having a different second surface direction and a different second surface orientation.

De Souza et al discloses bonding a first wafer having a first surface direction and a first surface orientation atop a second wafer having a different second surface direction and a different second surface orientation (Figure 6, references 170 and 180).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Bryant et al, with the teachings of De Souza et al, for the purpose of utilizing localized amorphization and recrystallization of stacked template layers for making a planar substrate having semiconductor layers of different crystallographic orientations.

19. Regarding claim 19, Bryant et al discloses wherein each wafer includes a silicon layer on an insulator layer (Figure 4), and the opening forming step includes forming the opening to the silicon layer of the second wafer (Figure 4, reference 70).

20. Regarding claim 20, Bryant et al discloses wherein the region generating step includes epitaxially growing silicon in the opening, and planarizing the silicon, and the opening forming step further includes forming a sidewall spacer along the opening (pg.4, paragraph 0064).

Response to Arguments

21. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Monica D. Harrison
AU 2813

mdh
June 25, 2007

Carl Whitehead
SPE 2814